

# 74LVTH162374

## Low Voltage 16-Bit D-Type Flip-Flop with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Power Down high impedance provides glitch-free bus loading
- Outputs include equivalent series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

### General Description

The LVTH162374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable ( $\overline{OE}$ ) are common to each byte and can be shorted together for full 16-bit operation.

The LVTH162374 is designed with equivalent 25Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162374 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These flip-flops are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH162374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

### Ordering Information

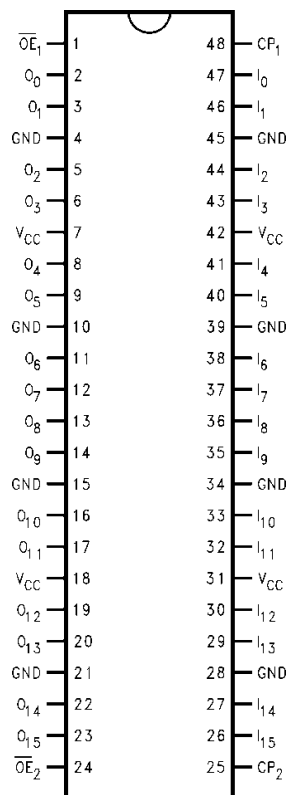
Order Number	Package Number	Pb-Free	Package Description	Supplied As
74LVTH162374GX <sup>(1)</sup>	BGA54A (Preliminary)	Yes	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide	Tape and Reel
74LVTH162374MEA	MS48A	Yes	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide	Tubes
74LVTH162374MEX	MS48A	Yes	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide	Tape and Reel
74LVTH162374MTD	MTD48	Yes	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide	Tubes
74LVTH162374MTX	MTD48	Yes	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide	Tape and Reel

#### Notes:

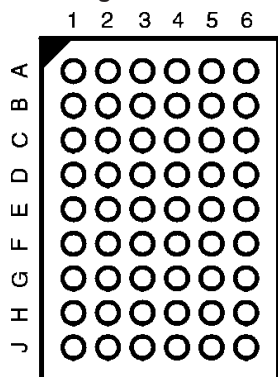
1. BGA package available in Tape and Reel only.

## Connection Diagrams

Pin Assignments for SSOP and TSSOP



Pin Assignment for FPGA



(Top Thru View)

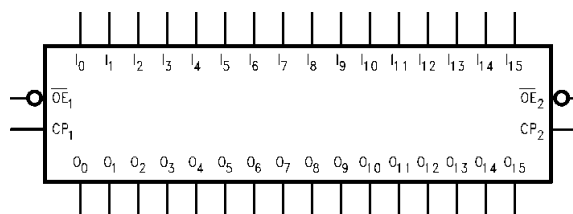
## Pin Description

Pin Name	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$CP_n$	Clock Pulse Input
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	3-STATE Outputs
NC	No Connect

## FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_0$	NC	$\overline{OE}_1$	$CP_1$	NC	$I_0$
<b>B</b>	$O_2$	$O_1$	NC	NC	$I_1$	$I_2$
<b>C</b>	$O_4$	$O_3$	$V_{CC}$	$V_{CC}$	$I_3$	$I_4$
<b>D</b>	$O_6$	$O_5$	GND	GND	$I_5$	$I_6$
<b>E</b>	$O_8$	$O_7$	GND	GND	$I_7$	$I_8$
<b>F</b>	$O_{10}$	$O_9$	GND	GND	$I_9$	$I_{10}$
<b>G</b>	$O_{12}$	$O_{11}$	$V_{CC}$	$V_{CC}$	$I_{11}$	$I_{12}$
<b>H</b>	$O_{14}$	$O_{13}$	NC	NC	$I_{13}$	$I_{14}$
<b>J</b>	$O_{15}$	NC	$\overline{OE}_2$	$CP_2$	NC	$I_{15}$

## Logic Symbol



## Truth Tables

Inputs			Outputs
$CP_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
↗	L	H	H
↗	L	L	L
L	L	X	$O_o$
X	H	X	Z

Inputs			Outputs
$CP_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_o$
X	H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = HIGH Impedance

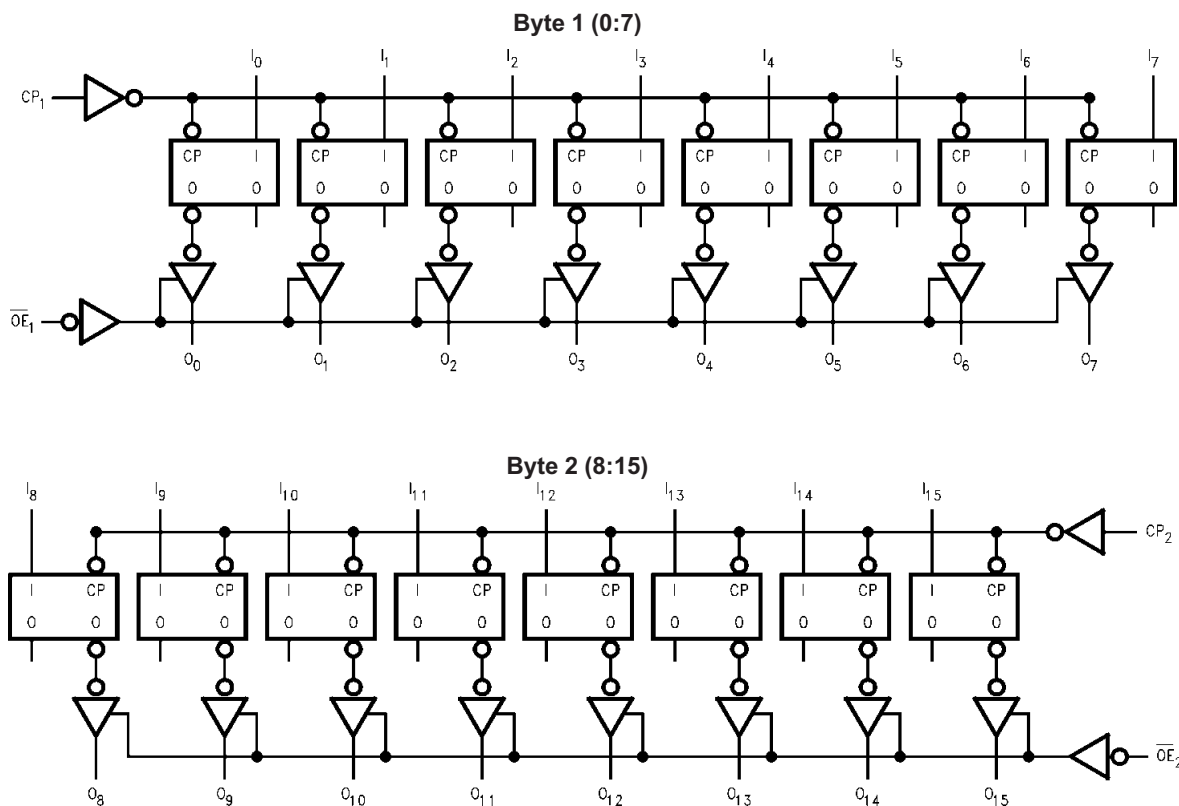
$O_o$  = Previous  $O_o$  before LOW-to-HIGH of CP

## Functional Description

The LVTH162374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each

flip-flop will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock ( $CP_n$ ) transition. With the Output Enable ( $\overline{OE}_n$ ) LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}_n$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}_n$  input does not affect the state of the flip-flops.

## Logic Diagrams



Please note that these diagrams are provided for the understanding of logic operation and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Value	Units
$V_{CC}$	Supply Voltage		-0.5 to +4.6	V
$V_I$	DC Input Voltage		-0.5 to +7.0	V
$V_O$	DC Output Voltage	Output in 3-STATE	-0.5 to +7.0	V
		Output in HIGH or LOW State <sup>(2)</sup>	-0.5 to +7.0	
$I_{IK}$	DC Input Diode Current	$V_I < GND$	-50	mA
$I_{OK}$	DC Output Diode Current	$V_O < GND$	-50	mA
$I_O$	DC Output Current	$V_O > V_{CC}$ Output at HIGH State	64	mA
		$V_O > V_{CC}$ Output at LOW State	128	
$I_{CC}$	DC Supply Current per Supply Pin		±64	mA
$I_{GND}$	DC Ground Current per Ground Pin		±128	mA
$T_{STG}$	Storage Temperature		-65 to +150	°C

### Note:

- $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_I$	Input Voltage	0	5.5	V
$I_{OH}$	HIGH Level Output Current		-12	mA
$I_{OL}$	LOW Level Output Current		12	mA
$T_A$	Free-Air Operating Temperature	-40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = -40°C to +85°C		Units	
				Min.	Max.		
V <sub>IK</sub>	Input Clamp Diode Voltage	2.7	I <sub>I</sub> = -18mA		-1.2	V	
V <sub>IH</sub>	Input HIGH Voltage	2.7–3.6	V <sub>O</sub> ≤ 0.1V or V <sub>O</sub> ≥ V <sub>CC</sub> – 0.1V	2.0		V	
V <sub>IL</sub>	Input LOW Voltage	2.7–3.6			0.8	V	
V <sub>OH</sub>	Output HIGH Voltage	2.7–3.6	I <sub>OH</sub> = -100μA	V <sub>CC</sub> – 0.2V		V	
		3.0	I <sub>OH</sub> = -12mA	2.0			
V <sub>OL</sub>	Output LOW Voltage	2.7	I <sub>OL</sub> = 100μA		0.2	V	
		3.0	I <sub>OL</sub> = 12mA		0.8		
I <sub>I(HOLD)</sub>	Bushold Input Minimum Drive	3.0	V <sub>I</sub> = 0.8V	75		μA	
			V <sub>I</sub> = 2.0V	-75			
I <sub>I(OD)</sub>	Bushold Input Over-Drive Current to Change State	3.0	(3)	500		μA	
			(4)	-500			
I <sub>I</sub>	Input Current	3.6	V <sub>I</sub> = 5.5V		10	μA	
			Control Pins	V <sub>I</sub> = 0V or V <sub>CC</sub>			±1
			Data Pins	V <sub>I</sub> = 0V			-5
				V <sub>I</sub> = V <sub>CC</sub>			1
I <sub>OFF</sub>	Power Off Leakage Current	0	0V ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V		±100	μA	
I <sub>PU/PD</sub>	Power Up/Down 3-STATE Output Current	0–1.5	V <sub>O</sub> = 0.5V to 3.0V, V <sub>I</sub> = GND or V <sub>CC</sub>		±100	μA	
I <sub>OZL</sub>	3-STATE Output Leakage Current	3.6	V <sub>O</sub> = 0.5V		-5	μA	
I <sub>OZH</sub>	3-STATE Output Leakage Current	3.6	V <sub>O</sub> = 3.0V		5	μA	
I <sub>OZH+</sub>	3-STATE Output Leakage Current	3.6	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V		10	μA	
I <sub>CCH</sub>	Power Supply Current	3.6	Outputs HIGH		0.19	mA	
I <sub>CCL</sub>	Power Supply Current	3.6	Outputs LOW		5	mA	
I <sub>CCZ</sub>	Power Supply Current	3.6	Outputs Disabled		0.19	mA	
I <sub>CCZ+</sub>	Power Supply Current	3.6	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled		0.19	mA	
ΔI <sub>CC</sub>	Increase in Power Supply Current <sup>(5)</sup>	3.6	One Input at V <sub>CC</sub> – 0.6V Other Inputs at V <sub>CC</sub> or GND		0.2	mA	

## Notes:

- An external driver must source at least the specified current to switch from LOW-to-HIGH.
- An external driver must sink at least the specified current to switch from HIGH-to-LOW.
- This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

**Dynamic Switching Characteristics<sup>(6)</sup>**

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	T <sub>A</sub> = -40°C to +85°C			Units
				Min.	Typ.	Max	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	(7)		0.8		V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	(7)		-0.8		V

**Note:**

6. Characterized in SSOP package. Guaranteed parameter, but not tested.  
7. Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω				Units
		V <sub>CC</sub> = 3.3V ±0.3V		V <sub>CC</sub> = 2.7V		
		Min.	Max.	Min.	Max.	
f <sub>MAX</sub>	Maximum Clock Frequency	160		150		MHz
t <sub>PHL</sub>	Propagation Delay, CP to On	2.0	5.1	2.0	5.3	ns
t <sub>PLH</sub>		1.6	5.3	1.6	6.2	
t <sub>PZL</sub>	Output Enable Time	1.8	5.0	1.8	6.0	ns
t <sub>PZH</sub>		1.2	5.6	1.2	6.9	
t <sub>PLZ</sub>	Output Disable Time	1.9	5.0	1.9 2.0	5.1	ns
t <sub>PHZ</sub>		2.0	5.4		5.7	
t <sub>S</sub>	Setup Time	1.8		2.0		ns
t <sub>H</sub>	Hold Time	0.8		0.1		ns
t <sub>W</sub>	Pulse Width	3.0		3.0		ns
t <sub>OSHL</sub>	Output to Output Skew <sup>(8)</sup>		1.0		1.0	ns
t <sub>OSLH</sub>			1.0		1.0	

**Note:**

8. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Capacitance<sup>(9)</sup>**

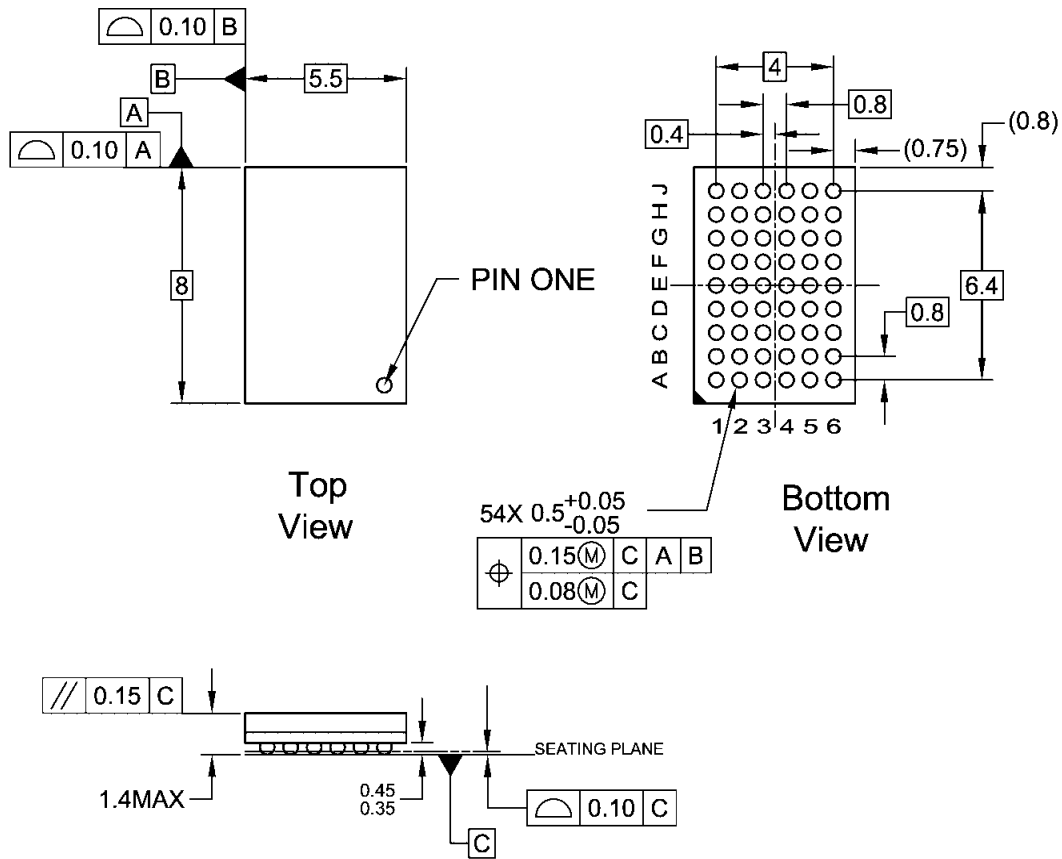
Symbol	Parameter	Conditions	Typ.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = OPEN, V <sub>I</sub> = 0V or V <sub>CC</sub>	4	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.0V, V <sub>O</sub> = 0V or V <sub>CC</sub>	8	pF

**Note:**

9. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

### Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



**NOTES:**

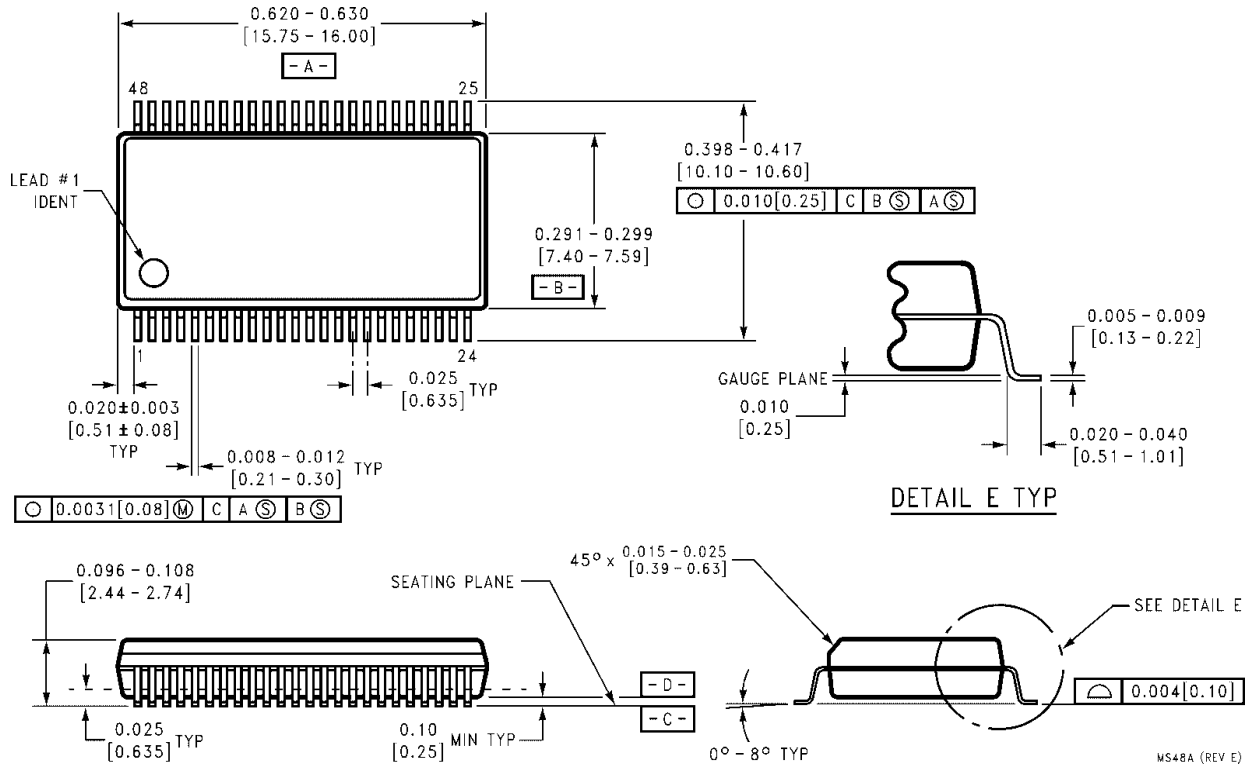
- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**Figure 1. 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A  
(Preliminary)**

**Physical Dimensions (Continued)**

Dimensions are in millimeters unless otherwise noted.

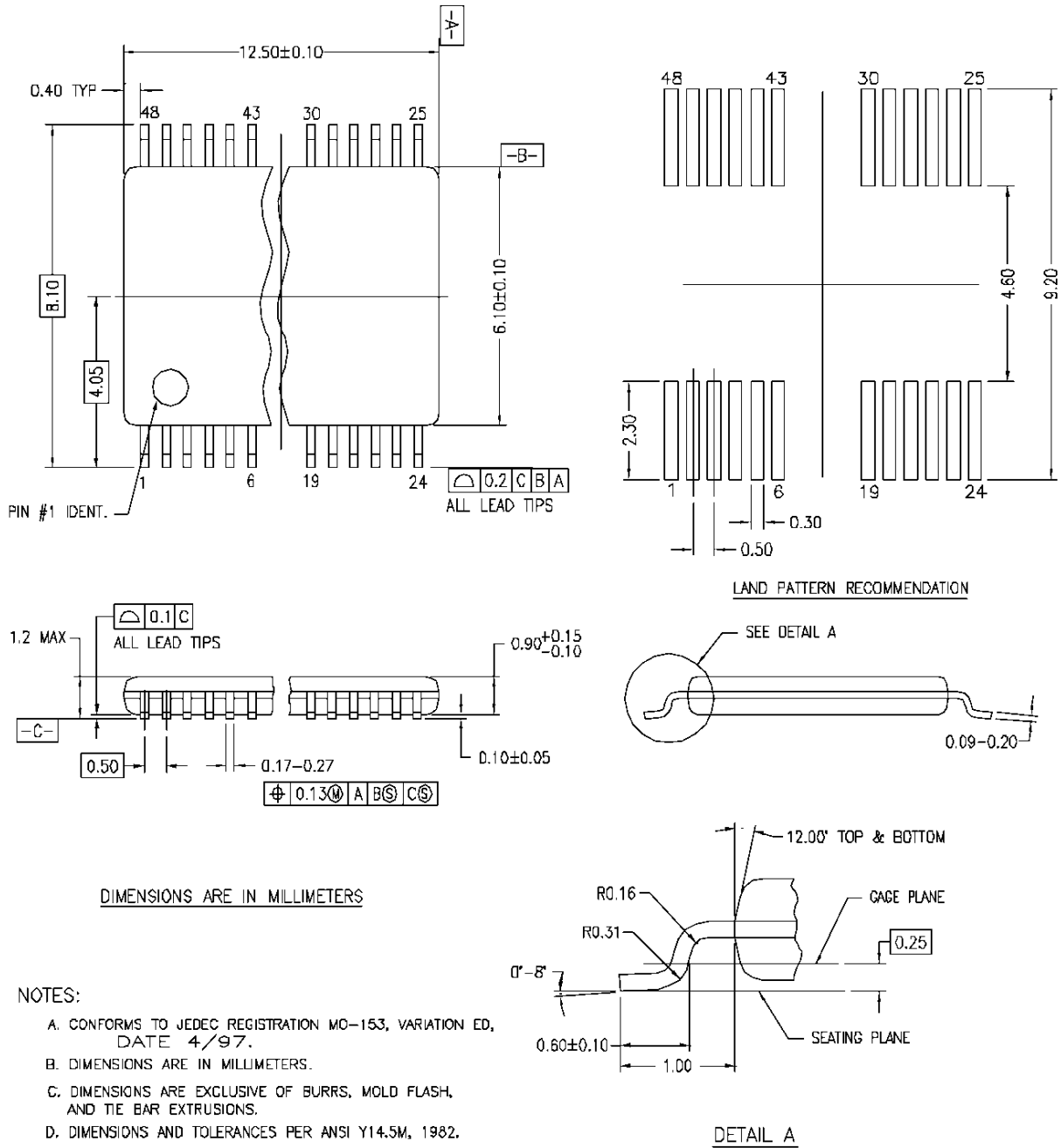


**Figure 2. 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide Package Number MS48A**



### Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.




MTD48REV C

**Figure 3. 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MDT48**



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<b>F</b> ®	MICROCOUPLER™	QT Optoelectronics™	TINYOPTO™
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FAST®	OPTOPLANAR®	STEALTH™	UHC®
FastvCore™	 ®	SuperFET™	UniFET™
FPS™	PDP-SPM™	SuperSOT™-3	VCX™
FRFET®	Power220®	SuperSOT™-6	
Global Power Resource <sup>SM</sup>			

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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. 130